Amendments to the Specification

Kindly amend the paragraph appearing at page 3, lines 5-9, to read as follows:

For example, the process is rather complex. Moreover, part of the gate upper dielectric layer 22 is consumed by polishing or etching during the CMP process for manufacturing the contact pad. This may result in shorting of the contact pad 34' and the silicide 24. This ultimately will result in shorting of the gate and bit line of the ~~semi-conductor~~ semiconductor device.

Kindly amend the paragraph appearing at page 3, lines 10-14, to read as follows:

Finally, in order to prevent the gate upper dielectric layer from becoming too thin, a relatively thick gate upper dielectric layer 22 may be formed. As such, the thickness of the interdielectric layer 16 must be increased. An increase in the thickness of the interdielectric layer may result in the ~~undesireable~~ undesirable formation of voids within the interdielectric layer.

Kindly amend the paragraph bridging pages 3 and 4 to read as follows:

According to an illustrative embodiment of the present invention, a method of fabricating a contact pad of a semiconductor device includes forming a gate structure including a gate upper dielectric layer on a semiconductor substrate; forming a stopping layer over the semiconductor substrate; forming an interdielectric layer over the stopping layer; planarizing the interdielectric layer to expose at least the gate upper dielectric layer using a material which ~~exhibit~~ exhibits a high-polishing selectivity with respect to the interdielectric layer; etching the interdielectric layer in a region in which a contact pad will be formed on the semiconductor substrate; depositing a conductive material on the semiconductor substrate; and planarizing using a material which exhibits a high-

polishing selectivity of the gate upper dielectric layer with respect to the conductive material.

Kindly amend the paragraph appearing at page 4, lines 8-17, to read as follows:

Advantageously, in the CMP process for planarizing the interdielectric layer and the conductive material for the contact pad according to an illustrative embodiment of the present invention, because a slurry is used which gives a high polishing selectivity of the interdielectric layer with respect to the conductive material for the contact pad to the gate upper dielectric layer, the process can be simplified, and the loss in thickness of the gate upper dielectric layer can be minimized. As such, electrical shorting of the gate and the bit line can be prevented, and the process margin can be improved. Also, since the thickness of the interdielectric layer can be reduced by reducing the thickness of the gate upper dielectric layer, the occurrence of voids can be suppressed.

Kindly amend the paragraph bridging pages 5 and 6 to read as follows:

Referring to FIG. 5, a gate structure 120 is formed on a semiconductor substrate 100 on which a device separating layer 102 is formed. The described gate structure 120 is illustratively formed of a gate electrode 126 of polysilicon, a silicide layer 124 of tungsten silicide (WSi_x) over the gate electrode 126, a gate upper dielectric layer 122 (e.g. a nitride layer, or an oxide aluminum layer (Al_2O_3)) over the silicide layer 124, and a gate spacer ~~124~~ 128 of a nitride layer on the side walls of the gate electrode 126, the silicide layer 124, and the gate upper dielectric layer 122.

Kindly amend the paragraph appearing at page 6, lines 4-15, to read as follows:

It is useful to form the gate upper dielectric layer 122 to an illustrative thickness in the range of approximately 1500 Å and 2500 Å; and particularly to a thickness of 2000 Å. Next, a stopping layer 104, for example, a nitride layer, is formed over the semiconductor substrate 100 by blanket deposition. Illustratively, the thickness of the stopping layer 104 is in the range of approximately 50 Å and 150 Å. Next, an interdielectric layer 106 is deposted over the stopping layer 104. The interdielectric layer 106 is illustratively a high density plasma oxide layer (HDP Oxide), a ~~spin-on-glass~~ spin-on-glass (SOG) layer, a boron phosphorous silicate glass (BPSG) layer, a phosphorous silicate glass (PSG) layer, an undoped silicate glass (USG) layer, a plasma enhanced tetra ethyl ortho silicate glass (PE-TEOS) layer, a flowable oxide (FOX) layer, a photoresister layer, or a polymer layer. The deposited interdielectric layer 106 may be planarized by reflowing.

Kindly amend the paragraph bridging pages 6 and 7 to read as follows:

Illustratively, when a chemical mechanical polishing (CMP) process is performed on the interdielectric layer 106, the gate upper dielectric layer 122 or the stopping layer 104 may be used as a polishing stopping layer for planarization. The interdielectric layer 106 can be relatively thin compared to the thickness of those required for conventional techniques describe above. The method for planarizing according to the illustrative embodiment of the present invention is performed using a slurry including abrasive particles which exhibit a polishing selectivity of the interdielectric layer 106 with respect to the gate upper dielectric layer 122 in the range of approximately 5:1 to approximately 50:1. Alternatively, planarizing can be performed by a dry etching method which exhibits an etch selectivity of the interdielectric layer 106 with respect to the gate upper dielectric layer 122 in the range of approximately 5:1 to approximately 50:1. That is, the planarization process is performed using a material which exhibits a high polishing selectivity relative to the material used for interdielectric layer 106; and which exhibits a low etching selectivity or a low polishing selectivity with respect

to the gate upper dielectric layer 122, which is illustratively a nitride. The slurry may be alumina, silica, ceria, or Mn_2O_3[[,]] particles. In the illustrative embodiment a slurry of a ceria base is used.

Kindly amend the paragraph appearing at page 8, lines 8-14, to read as follows:

Referring to FIG. 7, self aligned contact (SAC) etching is performed using the photoresist pattern 134 as an etching mask. Illustratively, a part of the interdielectric layer 106 of the region in which the contact pad will be formed 108 is removed by a conventional dry etching method. Thereafter, a part of the stopping layer 104 exposed to the region in which the contact pad will be formed ~~180~~ 108 is removed by ~~the~~ dry etching. In the above process, the anti-reflective layer 132 is removed with the photoresist pattern 134.

Kindly amend the paragraph appearing at page 8, lines 15-19, to read as follows:

The conductive material 136 for the contact pad (e.g. doped polysilicon) is deposited to cover the entire surface of the semiconductor substrate on which the region in which the contact pad will be formed 108 is etched. Illustratively, the conductive material 136 for the contact pad can also be ~~titanum~~ titanium, ~~titanum~~ titanium nitride, and tungsten.

Kindly amend the paragraph bridging pages 8 and 9 to read as follows:

According to the conventional process described above, dry etching is first performed and the conductive material 136 for the contact pad and some of the interdielectric layer are etched back. This is done to minimize the removal of the gate upper dielectric layer 122 by polishing in the following CMP process. This may also ~~improves~~ improve the uniformity of the CMP. However, in accordance

with the illustrative embodiment of the present invention, this process is not necessary.

Kindly amend the paragraph appearing at page 9, lines 6-13, to read as follows:

In the illustrative embodiment, if the chosen method for planarizing is a CMP process, a slurry is used which exhibits a high-polishing selectivity of the gate upper dielectric layer 122 over the conductive material 136 for the contact pad 136A, polysilicon. Illustratively, this etch selectivity is in the range of approximately 1:5 to approximatley 1:50. The slurry can ~~be a slurry including~~ include abrasive particles such as alumina, silica, ceria[[,]] and Mn_2O_3. Advantageously, planarization can be easily achieved without dishing on the contact pad having a shape separated by one CMP process.

Kindly amend the paragraph appearing at page 9, lines 14-18, to read as follows:

Therefore, according to the illustrative embodiment of the present invention, the process for forming the contact pad is simplified compared to the conventional technique described above. Moreover, the loss of the upper portion of the gate upper dielectric layer 122 by polishing or etching can be suppressed by using ~~the~~ a slurry having a high polishing ratio.

Kindly amend the paragraph appearing at page 10, lines 15-20, to read as follows:

In the graph, the symbol ~~"X"~~ "■" indicates the thickness of the gate upper dielectric layer measured after forming the contact pad of the semiconductor device according to the exemplary embodiment as shown in FIGS. 5 through 8, and the symbol ~~"O"~~ " " indicates the thickness of the gate upper dielectric layer

measured after manufacturing the contact pad of the semiconductor device according to the conventional art as shown in FIGS. 1 through 4.

Kindly amend the paragraph appearing at page 11, lines 3-17, to read as follows:

Finally, as can be appreciated, the above description is merely illustrative of the invention. As such, the present invention can be embodied in different ways without departing from the spirit and essential features of the invention. For example, in the above described illustrative embodiment, an anti-reflective layer is ~~a~~ an amorphous carbon layer, but it can be an organic anti-reflective layer such as an oxide nitride layer (SiON). Also, in the above described illustrative embodiment, a slurry used for polishing the interdielectric layer using a high polishing selectivity of a gate upper dielectric layer to the interdielectric layer has a ceria base, but the ceria base can be replaced with a silica base or a slurry including abrasive particles of alumina and Mn_2O_3. Also, a slurry used for polishing a conductive material for a contact pad using a high polishing selectivity of the gate upper dielectric layer and the conductive material for the contact pad has a silica base, but the silica base can be replaced with a ceria base, or a slurry including abrasive particles of alumina and Mn_2O_3. Of course, other variations and modifications in keeping with the teaching of the present invention are possible.